What is claimed is:

1. A frequency multiplier which receives an external clock signal having a predetermined frequency, multiplies the external clock signal, and outputs the multiplied signal as an internal clock signal, the frequency multiplier comprising:

a first pulse signal generating circuit which receives a first clock signal and a second clock signal that have the same frequency as each other and generates a first pulse signal having a first pulse width when the level of the first clock signal is greater than the level of the second clock signal;

a second pulse signal generating circuit which is enabled in response to a first control signal, receives a reference voltage and the first clock signal, and generates a second pulse signal having a second pulse width when the level of the reference voltage is greater than the level of the first clock signal; and

an OR circuit which receives the first pulse signal and the second pulse signal, logically sums the first pulse signal and the second pulse signal, and outputs the logically summed signal as the internal clock signal.

2. The frequency multiplier of claim 1, wherein the first pulse signal generating circuit further comprises:

a first differential amplifier which receives the first clock signal and the second clock signal, senses a difference between the first clock signal and the second clock signal, and amplifies the difference; and

a first logic circuit which receives an output signal of the first differential amplifier and generates the first pulse signal corresponding to the output signal of the first differential amplifier.

3. The frequency multiplier of claim 2, wherein the second pulse signal generating circuit further comprises:

a second differential amplifier which is enabled in response to the first control signal, receives a reference voltage and the first clock signal, senses a difference between the reference voltage and the first clock signal, and amplifies the difference; and

a second logic circuit which receives an output signal of the second differential amplifier and generates the second pulse signal corresponding to the output signal of the second differential amplifier.

4. The frequency multiplier of claim 3, wherein the first control signal is enabled in a dual edge mode.

5. The frequency multiplier of claim 1, wherein the first pulse signal and the second pulse signal have the same pulse width.

6. A frequency multiplier which receives an external clock signal having a predetermined frequency, multiplies the external clock signal, and outputs the multiplied signal as an internal clock signal, the frequency multiplier comprising:

a first pulse signal generating circuit which receives a first clock signal and a second clock signal having the same frequency and outputs a first pulse signal having a first pulse width when the level of the first clock signal is greater than the level of the second clock signal;

a second pulse signal generating circuit which is enabled in response to a first control signal and outputs a second pulse signal having a second pulse width when the level of the reference voltage is greater than the level of the first clock signal;

a third pulse signal generating circuit which is enabled in response to a second control signal and the reference voltage and outputs a third pulse signal having a third pulse width when the level of the second clock signal is greater than the level of the reference voltage;

a fourth pulse signal generating circuit which is enabled in response to a second control signal, receives the reference voltage and the second control signal, and outputs a fourth pulse signal having a fourth pulse width when the level of the reference voltage is greater than the level of the second clock signal; and

an OR circuit which receives the first pulse signal, the second pulse signal, the third pulse signal, and the fourth pulse signal, and outputs the internal clock signal which is the logical sum of the first pulse signal, the second pulse signal, the third pulse signal, and the fourth pulse signal.

7. The frequency multiplier of claim 6, wherein the first pulse signal generating circuit further comprises:

a first differential amplifier which receives the first clock signal and the second clock signal, senses a difference between the first clock signal and the second clock signal, and amplifies the difference; and

a first logic circuit which receives an output signal of the first differential amplifier and generates the first pulse signal corresponding to the output signal of the first differential amplifier.

8. The frequency multiplier of claim 7, wherein the second pulse signal generating circuit further comprises:

a second differential amplifier which is enabled in response to the first control signal, receives the reference voltage and the first clock signal, senses a difference between the reference voltage and the first clock signal, and amplifies the difference;

a second logic circuit which receives an output signal of the second differential amplifier and generates the second pulse signal corresponding to the output signal of the second differential amplifier.

9. The frequency multiplier of claim 8, wherein the third pulse signal generating circuit further comprises:

a third differential amplifier which is enabled in response to the second control signal, receives the second clock signal and the reference voltage, senses a difference between the second clock signal and the reference voltage, and amplifies the difference; and

a third logic circuit which receives an output signal of the third differential amplifier and generates the third pulse signal corresponding the output signal of the third differential amplifier.

10. The frequency multiplier of claim 9, wherein the fourth pulse signal generating circuit further comprises:

a fourth differential amplifier which is enabled in response to the second control signal, receives the reference voltage and the second clock signal, senses the

difference between the reference voltage and the second clock signal, and amplifies the difference; and

a fourth logic circuit which receives an output signal of the fourth differential amplifier and generates the fourth pulse signal corresponding to the output signal of the fourth differential amplifier.

11. The frequency multiplier of claim 6, wherein the first pulse signal, the second pulse signal, the third pulse signal, and the fourth pulse signal have the same pulse width as each other.

12. The frequency multiplier of claim 6, wherein the first control signal is enabled in a dual edge mode, and the second control signal is enabled in a quadrature edge mode.

13. A data output buffer of a semiconductor device comprising:

N flip flops which receive a first clock signal, are connected in series to each other, including a first flip flop that receives data to be output from the semiconductor device, is synchronized with the first clock signal, and outputs the data, and second through Nth flip flops that each receive an output signal of the preceding flip flop in the series, is synchronized with the first clock signal, and outputs the output signal of the preceding flip flop;

an OR circuit which receives output signals from the N flip flops, logically sums the output signals, and outputs the signal obtained by the summation; and

an output circuit which is synchronized with a second clock signal and outputs the output signal of the OR circuit,

wherein the clock signal frequency of the first clock signal is N times greater than the clock signal frequency of the second clock signal.

14. The data output buffer of claim 13, wherein the data output buffer includes 4 flip flops which are connected in series with each other.

15. The data output buffer of claim 14, wherein the first clock signal has a frequency 4 times greater than the second clock signal.

16. A semiconductor device comprising:

a frequency multiplier which is placed in an input terminal of the semiconductor device, receives a clock signal having a predetermined frequency, and outputs an internal clock signal having greater frequency than the predetermined frequency; and

a data output buffer which outputs data tested according to data written to test the semiconductor device,

wherein the frequency multiplier comprises:

a first pulse signal generating circuit which receives a first clock signal and a second clock signal having the same frequency and outputs a first pulse signal having a first pulse width when the level of the first clock signal is greater than the level of the second clock signal;

a second pulse signal generating circuit which is enabled in response to a first control signal and outputs a second pulse signal having a second pulse width when the level of the reference voltage is greater than the level of the first clock signal;

a third pulse signal generating circuit which is enabled in response to a second control signal and the reference voltage and outputs a third pulse signal having a third pulse width when the level of the second clock signal is greater than the level of the reference voltage;

a fourth pulse signal generating circuit which is enabled in response to a second control signal, receives the reference voltage and the second control signal, and outputs a fourth pulse signal having a fourth pulse width when the level of the reference voltage is greater than the level of the second clock signal; and

an OR circuit which receives the first pulse signal, the second pulse signal, the third pulse signal, and the fourth pulse signal and outputs the internal clock signal which is the logical sum of the first pulse signal, the second pulse signal, the third pulse signal, and the fourth pulse signal.

17. The semiconductor device of claim 16, wherein the first pulse signal, the second pulse signal, the third pulse signal, and the fourth pulse signal have the same pulse width.

18. The semiconductor device of claim 17, wherein the first control signal is enabled in a dual edge mode and the second control signal is enabled in a quadrature edge mode.

19. The semiconductor device of claim 18, wherein the data output buffer comprises:

N flip flops which receive a first clock signal, are connected in series to each other, including a first flip flop that receives data to be output from the semiconductor device, is synchronized with the first clock signal, and outputs the data, and second through Nth flip flops that each receive an output signal of the preceding flip flop in the series, is synchronized with the first clock signal, and outputs the output signal of the preceding flip flop;

an OR circuit which receives output signals from the N flip flops, logically sums the output signals, and outputs the signal obtained by the summation; and

an output circuit which is synchronized with a second clock signal and outputs the output signal of the OR circuit,

wherein the clock signal frequency of the first clock signal is N times greater than the clock signal frequency of the second clock signal.

20. The semiconductor device of claim 19, wherein the data output buffer includes 4 flip flops which are connected in series with each other.

21. The semiconductor device of claim 20, wherein the first clock signal has a frequency 4 times greater than the second clock signal.

22. A method of multiplying a frequency where a clock signal having a predetermined frequency is received, the received clock signal is multiplied, and the multiplied signal is output as an internal signal, the method comprising:

generating a first pulse signal, which receives a first clock signal and a second clock signal and which has a first pulse width, when a level of the first clock signal is greater than a level of the second clock signal;

generating a second pulse signal which is enabled in response to a first control signal, and has a second pulse width, when the level of a received reference voltage is greater than the level of the first clock signal; and

receiving the first pulse signal and the second pulse signal, logically summing the first pulse signal and the second pulse signal, and outputting the signal obtained by the summation as the internal clock signal.

23. The method of claim 22, wherein the first control signal is enabled in a dual edge mode.

24. The method of claim 22, wherein the first pulse signal and the second pulse signal have the same pulse width as each other.

25. A method of multiplying a frequency where a clock signal having a predetermined frequency is received, the received clock signal is multiplied, and the multiplied signal is output as an internal signal, the method comprising:

generating a first pulse signal, which receives a first clock signal and a second clock signal which has the same frequency and has a first pulse width, when the level of the first clock signal is greater than the level of the second clock signal;

generating a second pulse signal which is enabled in response to a first control signal and has a second pulse width, when the level of a received reference voltage is greater than the level of the first clock signal;

generating a third pulse signal which is enabled in response to the second control signal and the reference voltage and has a third pulse width when a level of the second clock signal is greater than a level of the reference voltage;

generating a fourth pulse signal which is enabled in response to a second control signal, and has a fourth pulse width, when the level of the reference voltage is greater than the level of the second clock signal; and

receiving the first pulse signal, the second pulse signal, the third pulse signal, and the fourth pulse signal and outputting the internal clock signal which is the logical sum of the first pulse, the second pulse signal, the third pulse signal, and the fourth pulse signal.

26. The method of claim 25, wherein the first pulse signal, the second pulse signal, the third pulse signal, and the fourth pulse signal have the same width.

27. The method of claim 25, wherein the first control signal is enabled in a dual edge mode, and the second control signal is enabled in a quadrature edge mode.